Chapter 5

Analog Constraints

5.1 Introduction

Noise: the interference of unwanted signals with information. Noise differentiates analog from digital circuits. A properly designed digital circuit is immune to noise, but analog circuits must account for noise if the circuit is to function with the desired performance. All analog constraints in physical design arise from noise. Additive noise can arise from many sources such as thermal noise, coupling parasitics, and device mismatching.

In this chapter, we will present algorithms for the consideration of analog constraints during placement. Here, we will consider noise generated from thermal mismatching, device mismatching, parasitic devices, and coupling parasitics.

5.2 Previous Work

Relatively little work has been done for analog constraints. The most extensive work has been performed at the cell level. The OPASYN system created the physical layout for CMOS operational amplifiers [121]. In this system, a circuit topology is selected from a database based on the user's specifications. The circuit's parameters, including *W/L* ratios, are determined using a gradient method [120]. The physical layout is generated using a floorplanning tool limited to slicing tree placements. Each device becomes a macro to be placed. The macros are detailed-routed using the Mighty switchbox router [207]. The final layout is compacted using SPARCS, a one-dimensional graph-based compactor [19].

The ANAGRAM system also utilizes the macro cell design style [74]. Module generation techniques are used to create the individual components and to preserve critical

matchings and symmetries. A simulated annealing-based placement algorithm places the components. The cost function includes terms to minimize total area, wire length and cell overlap. The ANAGRAM system uses a line-expansion router which accounts for crosstalk interaction between signals. ANAGRAM classifies signal nodes into three categories: *neutral*, *noisy*, and *sensitive*. Neutral nodes are low impedance, small voltage swing nodes which do not couple noise. Typically, neutral nodes are bias and power supply lines. Noisy nodes typically exhibit large voltage swings with relatively fast transition times. Circuit performance will be degraded if noise is coupled into a sensitive node. The input nodes of a high-gain stage are examples of sensitive nodes. The router attempts to minimize the crosstalk by computing a crosstalk penalty for each segment appended to the partial route. The total cost for a segment is

$$C = W + I \tag{5.1}$$

where W is the conventional incremental cost of a segment (proportional to its length, via cost etc.), and I is the crosstalk penalty. The crosstalk penalty is proportional to the length of overlap if a noisy and sensitive segment overlap. If a noisy and sensitive segment run parallel for a distance L at a separation D, the penalty is proportional to L/D^2 (unless a neutral segment occurs between the noisy and sensitive net segments). The neutral net shields the interaction. A ripup-and-reroute scheme is used to overcome the net ordering problem.

Recently, the ANAGRAM system has been enhanced [35][36]. New placement algorithms handle layout symmetries, allow dynamic merging of individual devices, and generate well contacts. Other enhancements include a k-bend routing algorithm which tentatively routes each net during a simulated annealing placement algorithm. Unfortunately, the large time complexity of this method makes it impractical for large circuits.

Geoffrey Wong presented an analog placement system based on simulated annealing [240]. In addition to the wire length cost, thermal, proximity, and isolation costs were inte-

grated into the objective function. All new configurations generated obey symmetry constraints (if any) between devices. The thermal cost for all power dissipaters was

$$C_T = \sum \frac{P_j x}{1 + y + X} \tag{5.2}$$

where x is the distance between the thermal symmetry line and the thermal dissipater, y is the distance between the thermal dissipater and the sensitive modules, X is the sensitive module separation distance, and P_j is the power dissipated by component j. This is shown in Figure 5.1.

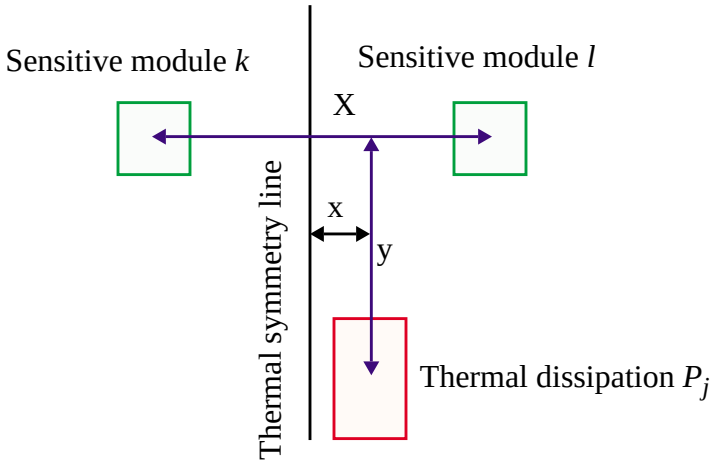

Figure 5.1 Definitions for thermal cost.

The costs for isolation C_I and proximity C_p of devices are given by

$$C_I = X + Y - (x - y) \tag{5.3}$$

and

$$C_p = x + y \tag{5.4}$$

where x and y represent the half perimeter of the bounding box of the two modules, and X and Y represent the half perimeter of the core region as shown in Figure 5.2.

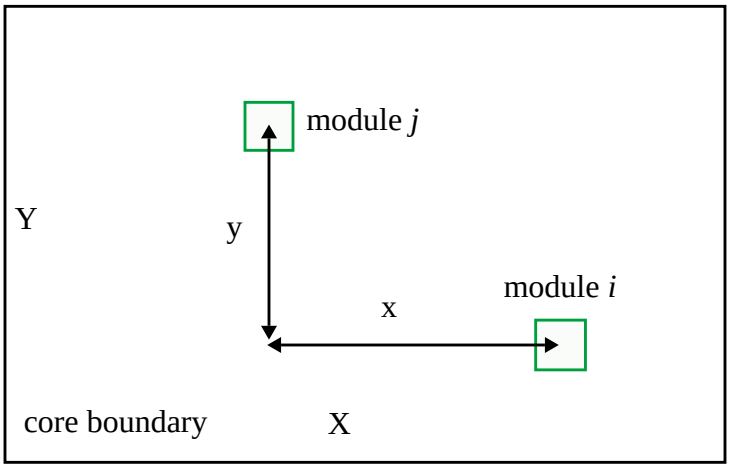

Figure 5.2 Definitions for isolation and proximity constraints.

The thermal cost metric reflects the strategy used by human designers. This metric yields favorable results without resorting to the computational expensive method of finite element analysis [68]. It will also be incorporated into our work as well.

The proximity and isolation metrics were included in the cost function to penalize crosstalk between modules. However, crosstalk does not only occur between modules, but also between the signal segments connecting the modules. In addition, this work does not have a provision for matching the lengths of conductors.

Charbon et al. introduced another simulated annealing placement algorithm which automatically translated electrical performance specifications into constraints on parasitics [28]. The constraints and sensitivity information of the circuit are used to control a simulated annealing placement algorithm. The simulated annealing objective function consists of seven components:

$$C(s) = \alpha_{wl} f_{wl}(s) + \alpha_a f_a(s) + \alpha_{ov} f_{ov}(s) + \alpha_{sy} f_{sy}(s) + \alpha_{ma} f_{ma}(s) + \alpha_{we} f_{we}(s) + \alpha_{co} f_{co}(s) \quad (5.5)$$

where f_{wl} is the wire length estimated using spanning trees, f_a is the total area of the circuit, f_{ov} is an overlap penalty, f_{sy} is a symmetry penalty, f_{ma} is a mismatch penalty, f_{we} is a

well discontinuity penalty, f_{co} is a performance constraint penalty. The performance penalty is computed as the sum of the contributions due to the violations of all constraints:

$$f_{co} = \sum_{i=1}^{N_c} C_{K_i} \tag{5.6}$$

where C_{K_i} is given by

$$_{K_i} = \begin{cases} 0 & \text{if} \quad \Delta K_i^{max} \leq \overline{\Delta K_i} \\ \Delta K_i^{max} - \overline{\Delta K_i} & \text{if} \quad \Delta K_i^{min} < \overline{\Delta K_i} \leq \Delta K_i^{max} \\ (S_r + 1)\left(\Delta K_i^{max} - (S_r \rho_c + 1)\, \overline{\Delta K_i} \right) & \text{if} \quad \overline{\Delta K_i} \leq \Delta K_i^{min} \end{cases} \tag{5.7}$$

and K_i is the *ith* performance metric, ΔK_i is the degradation of its performance, ρ_c is the ratio of the maximum to minimum parasitic capacitance, and S_r is a constant.

This method has the advantage of explicitly referencing the performance specification of the circuit. However, this has more than tripled the CPU time and is infeasible for designs that are much larger than small analog circuits. In addition, the symmetry and matching constraints should not be in the cost function. Symmetry and matching constraints are more effectively and more easily enforced by the move generation algorithm as proposed in the ANAGRAM II system.

Another method for analog layout automation is based on the semi-custom row based style. Several systems try to accommodate the analog constraints using standard analog cells [226]. In the LTX2 system, analog cells and digital cells were partitioned [57][111]. The bias and tub supplies were routed along the edge of the analog standard cells to form a shield between sensitive analog nets and large-swing digital nets. During detailed-routing, poly widths were increased to maintain accurate resistance. Interactions between the digital and analog sections were ignored; the satisfaction of the constraints was achieved at the expense of adding extra space to shield nets.

Unfortunately, most of these algorithms are unable to automatically process large systems consisting of analog and digital circuits[1]. In the future, integrated circuits will contain large digital processors combined with small analog sections for analog to digital (A/D) and digital to analog (D/A) processing. For this reason, we will concentrate on placement constraints which control the interaction between analog and digital circuitry, specifically net and crosstalk constraints.

5.3 Net Constraints

An important analog signal constraint is the matching of path lengths. On occasion, it is desirable to match the lengths of two paths. For example, the paths from the bond pad to the differential input pair of an operational amplifier should be matched to avoid offset errors. All net constraints enter the simulated annealing cost function through the timing penalty function. The user specifies a tolerance for the mismatch in path length. The penalty for a pair of paths p is given by

$$_p = \begin{cases} match(p) - tolerance(p) & \text{if } match(p) > tolerance(p) \\ 0 & \text{otherwise} \end{cases} \tag{5.8}$$

where the match is defined as

$$match(p) = \left| length(p_1) - length(p_2) \right| \tag{5.9}$$

where p_1 and p_2 are the two paths in p and length is measured using the half-perimeter bounding box,

$$length(p_i) = \sum_{\forall n \in p_i} S_x(n) + S_y(n) . \tag{5.10}$$

The timing penalty will be discussed in detail in Chapter 6.

1. The LTX2 system is the exception.

5.4 Crosstalk Constraints

Crosstalk or parasitic coupling between two signals limits the performance of analog circuits. When the wire segments of the two signals (segments *A* and *B*) are in close proximity for long distances, a parasitic capacitor is formed between them whose value is approximately,

$$C_{AB} = \frac{\varepsilon A}{d} \tag{5.11}$$

where *A* is the area of the overlapping segments, *d* is the distance between the segments, and ε is the permittivity of silicon dioxide. This parasitic capacitor will interfere with the desired circuit behavior if segment *A* carries a signal with sharp transitions. The high frequency content of a sharp transition will be injected into segment *B* if the value of the capacitor is large. The coupling problem can be alleviated if the nets are physically separated. The separation may be accomplished in two ways: the distance between conductors is increased, or the area of overlap is decreased.

General net classification	ANAGRAM net classification
NET digital_net1 CLASS 1	NET digital_net1 noisy
NET analog_net1 CLASS 2	NET analog_net1 sensitive
NET ground CLASS 3	NET ground CLASS neutral
NET digital_net2 CLASS 4	NET digital_net2 CLASS noisy
NET digital_net3 CLASS 5	NET digital_net3 CLASS noisy
CROSSTALK CLASS 1 CLASS 2 10 10	
CLASS 3 SHIELDS 1 FROM 2	
CROSSTALK CLASS 2 CLASS 4 20 20	
CROSSTALK CLASS 4 CLASS 5 20 20	

Figure 5.3 General net classification for crosstalk versus ANAGRAM's net classification.

In order to add crosstalk constraints to the layout problem, we allow the definition of net classes. Each net is assigned a class by the user. Coupling between signals are speci-

fied through crosstalk constraints. The minimum separation distance between net classes is specified for each direction as shown in Figure 5.3. In addition, some nets such as power and ground may act as shields for other net classes minimizing or eliminating crosstalk interactions. ANAGRAM's net classification scheme only allowed a net to belong in a single class. This classification scheme can not adequately represent the signal interaction in Figure 5.4. Each signal has a period of activity. In this case, only digital signals 1 and 2 interact with analog signal 1. In addition, digital signals 2 and 3 have common activity times. ANAGRAM's scheme constrains all signal combinations. This over-constrains the placement and global routing problems. The new generalized classification scheme correctly represents the interactions.

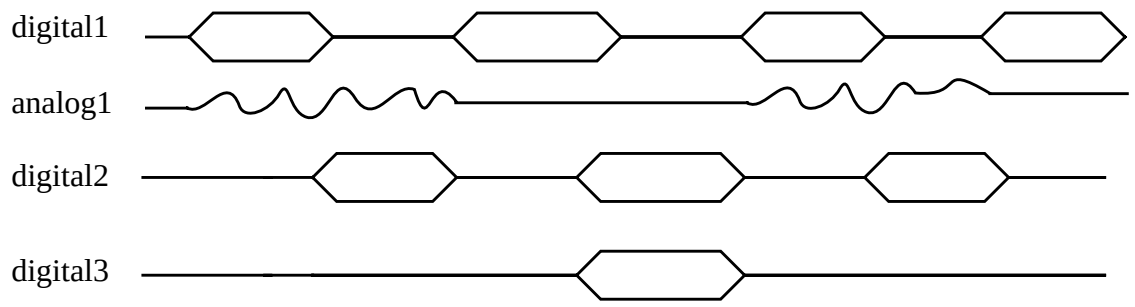

Figure 5.4 Signal waveforms for net classification. Each signal has a period of activity.

Crosstalk may be reduced during placement by adding a term to the simulated annealing cost function. The crosstalk penalty between two interacting nets *i* and *j* is the amount of overlap of their bounding boxes, or,

$$CT = \begin{cases} P_{ij} & \text{if overlap} \\ 0 & \text{otherwise} \end{cases} \tag{5.12}$$

$$P_{ij} = [\min(X_i, X_j) - \max(x_i, x_j)] + [\min(Y_i, Y_j) - \max(y_i, y_j)] + d_x + d_y \tag{5.13}$$

where d_x and d_y are the minimum required separations, and the coordinate system is defined in Figure 5.5.

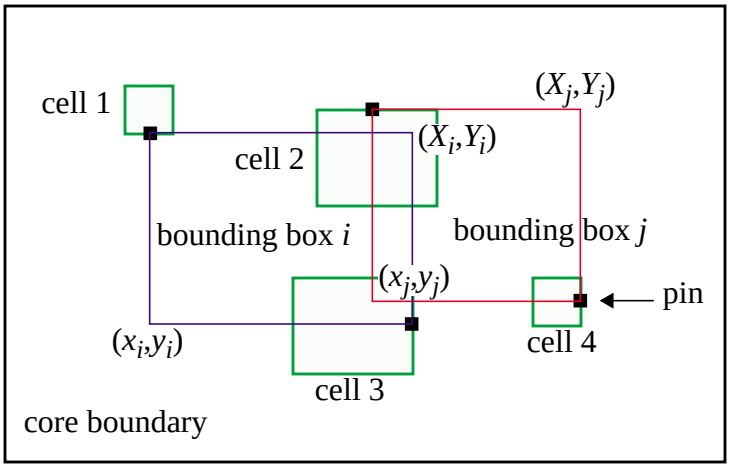

Figure 5.5 Definitions for crosstalk penalty.

In placement, the effects of shielding nets can not be accounted for without resorting to techniques such as *k*-bend detailed routing. However, shielding nets only improve the situation. The metric of Equation 5.12 adequately constrains the placement without a noticeable increase in execution time.

5.5 Results

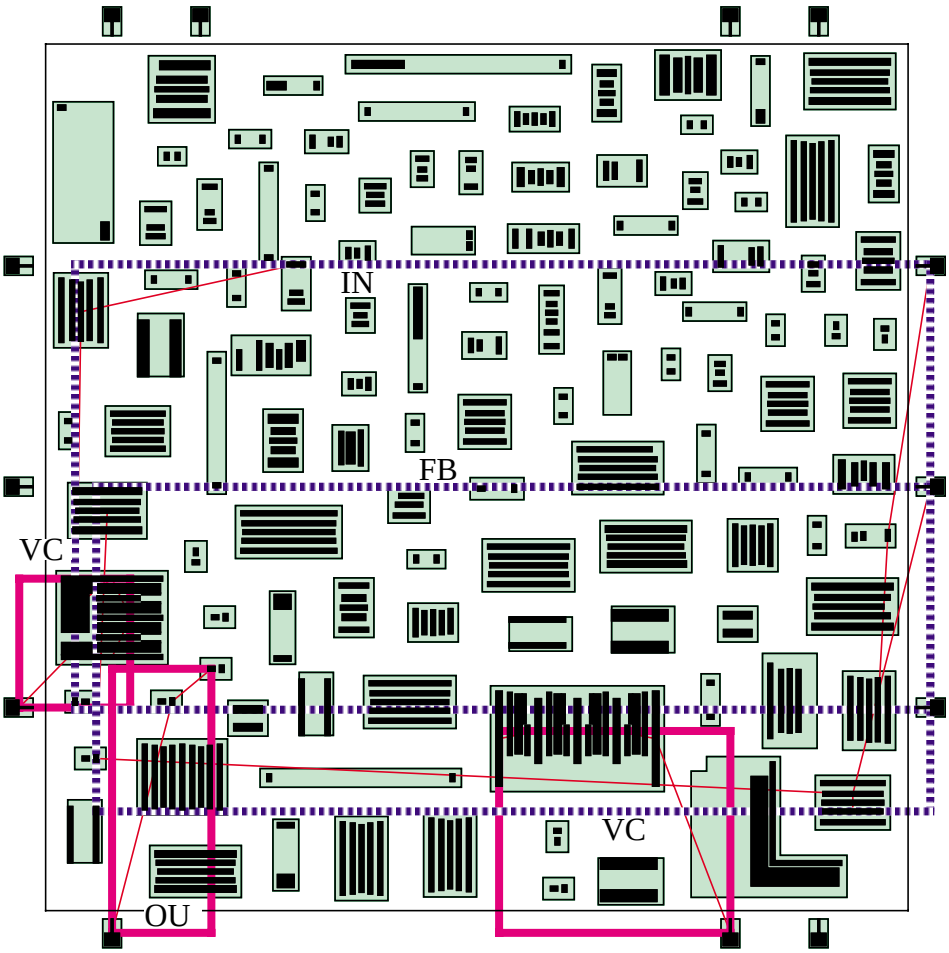

Figure 5.6 Harris 5004 op-amp without any constraints. Solid bounding boxes denote output class and dashed lines denote input class. Bounding boxes grossly overlap.

The algorithm was tested on a large operational amplifier. This amplifier is an order of magnitude larger than the six transistor op-amps tested in the literature. In this circuit, it was desired to separate the sensitive input nodes from the output nodes. The input nodes were put in the first net class; the output nodes in a second class. Without any net interaction constraints, the net bounding boxes of the signal classes overlapped creating significant crosstalk as shown in Figure 5.6. With the introduction of constraints, the crosstalk was completely eliminated as shown in Figure 5.7. This algorithm was capable of eliminating crosstalk without resorting to detailed-routing during placement. In addition, the

increase in execution time was negligible. This will allow application to much larger circuits.

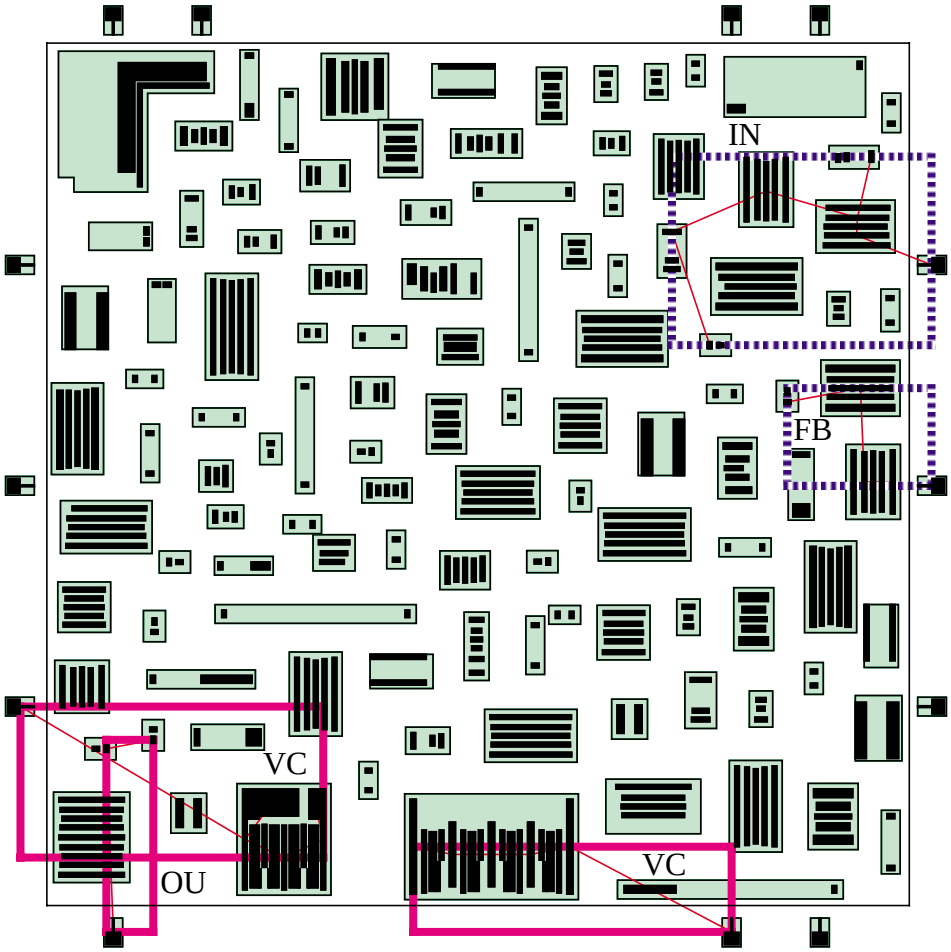

Figure 5.7 Harris 5004 op-amp with crosstalk constraints. Solid bounding boxes denote output class and dashed lines denote input class. Crosstalk has been completely eliminated.

5.6 Conclusions

In this chapter, we have presented a new general net classification scheme for eliminating crosstalk between signals. This has application in the placement of designs containing both analog and digital circuitry.